

## ABSTRACT

An addition circuit for digital data includes a digital adder for the addition of digital input data values present at data inputs of the digital adder to form a summation output data value, at an output of the digital adder. The data inputs have a predetermined data bit width  $n$ . A saturation circuit for limits the summation output data value present at a data input of the saturation circuit to be within a range determined by an upper threshold data value and a lower threshold data value. The  $n-m$  least significant data bits of the summation output data value are present directly at the data input of the saturation circuit, whereas the  $m$  most significant data bits of the summation output data value are switched through to the data input of the saturation circuit via a clock-state-controlled latch register.

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